AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 3 with the following amended paragraph:

[0003] One voltage source typically drives the input signals, the select signals, and the output signal. Generation of the output signal[[,]] typically results in a propagation delay, which increases the desired phase of the output signal. This non-zero propagation delay can impede the high speed performance of a phase mixer.

Please replace paragraph 21 with the following amended paragraph:

[0021] Each of driving blocks 110 and 112 can include the circuitry shown in FIG. 2. Driving block 200 receives an input signal 202 (e.g., signal 102 or 104), a select signal 204, and complement select signal 204' (e.g., signals 106/106' or 108/108'). Select signal 204 and its complement signal 204' can each have N select bits. Driving block 200 includes a driving unit 210. The number of driving units 210 can be the number of bits (e.g., N) in select signal 204 or another number. Each driving unit 210 includes two p-channel metal-oxide semiconductor (PMOS) transistors 212 and 214 and two n-channel metal-oxide semiconductor (NMOS) transistors 216 and 218 connected in series between a power voltage 220 and a ground voltage 222. The gate of PMOS transistor 212 is coupled to receive one of the bits of complement signal 204' while the source is connected to power voltage 220. The gate of NMOS transistor 218 is coupled to receive a corresponding bit of select signal 204 while the source is connected to ground voltage 222. The gates of PMOS transistor 214 and NMOS transistor 216 in each driving unit 210 are coupled to an input node 202 while the drains are tied

to an output node 224. (A signal received at node 202 will hereinafter be referred to as signal 202 while a signal output from node 224 will hereinafter be referred to as signal 224.)